## AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

**Listing of Claims:**

1. (currently amended) An apparatus comprising:

a ~~first~~ scanning dynamic logic circuit ~~having an output node on which a scan value is provided during scan~~ arranged serially to scan in a test value, in which the test value is to be scanned into a dynamic node of a first stage, propagated through subsequent stages and a resultant scanned sample output to be obtained from an output stage of the scanning dynamic logic circuit; and

~~one or more second dynamic logic circuits, wherein one of the second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, and wherein an output of the second dynamic logic circuits is sampled in response to the scan value during scan~~

a clock buffer circuit coupled to the scanning dynamic logic circuit to generate a first, second and third clock signals in response to a scan clock signal to clock a scan operation and a scan mode signal to indicate activation of the scan operation; wherein the first clock signal is to control a precharge cycle of the first stage, the second clock signal is to control an evaluate cycle of the first stage and the third clock signal is to control both precharge and evaluate cycles of remaining stages of the scanning dynamic logic circuit, the first and second clock signals to isolate the first stage from dynamic operation while the subsequent stages dynamically propagate the test value.

2-3. (canceled)

4. (currently amended) The apparatus as recited in claim ~~2~~ 1 further comprising a clocked storage device ~~configured~~ coupled to the output stage of the scanning dynamic logic circuit to sample the output ~~of the second dynamic logic circuits, wherein the clocked storage device is clocked by a fourth clock~~.

5. (currently amended) The apparatus as recited in claim ~~2~~ 4 wherein the ~~circuitry comprises a second clock buffer circuit configured to generate the second clock and a third clock buffer circuit configured to generate the third clock~~ clock buffer circuit to generate a fourth clock signal to clock the clocked storage device.

6. (currently amended) The apparatus as recited in claim ~~5~~ 1 wherein the ~~third~~ clock buffer circuit ~~comprises:~~ includes separate clock generation circuits to generate the first, second and third clock signals, wherein each clock generation circuit comprises transistors having programmable inputs in which signals coupled to the programmable inputs determine which of the first, second or third clock signals are generated

~~a series connection of transistors coupled between a first node and ground, the series connection of transistors including at least a first transistor and a second transistor, wherein the first transistor has a first control node coupled to receive a first signal corresponding to a functional clock and the second transistor has a second control node;~~

~~a logic circuit coupled to the second control node and coupled to receive the first signal and the scan mode signal, the logic circuit configured to deactivate the second transistor responsive to the scan mode signal indicating that scan is active~~.

7. (currently amended) The apparatus as recited in claim 6 wherein ~~the logic circuit is further configured to control the second transistor responsive to the first signal if the scan mode signal indicates that scan is inactive~~ each clock generation circuit includes a first and second programmable transistors, wherein coupling a first potential to gate input of the first transistor and the scan mode signal to gate input of the second transistor generates the first clock signal and coupling the first potential to gate input of the second transistor and the scan mode signal to gate input of the first transistor generates the second clock signal.

8. (currently amended) The apparatus as recited in claim ~~5~~ 7 wherein coupling the first potential to gate inputs of both the first and second transistors generates the third clock signal ~~the second clock buffer circuit comprises:~~

~~a series connection of transistors coupled between a first node and ground, the~~

~~series connection of transistors including at least a first transistor and a second transistor, wherein the first transistor has a first control node coupled to receive a first signal corresponding to a functional clock and the second transistor has a second control node controlled by an inverse of the first signal, the functional clock operating during functional operation;~~

~~a third transistor coupled to the first node, the third transistor having a third control node coupled to receive the scan mode signal~~.

9. (currently amended) The apparatus as recited in claim ~~8~~ 7 ~~further comprising a logic circuit coupled to receive the functional clock and the scan mode signal, wherein the logic circuit is configured to generate the first signal~~ wherein coupling the scan mode signal to gate input of the first transistor and the scan clock signal to gate input of the second transistor generates the third clock signal.

10. (currently amended) The apparatus as recited in claim 8 wherein the ~~first signal is further coupled to a fourth control node of a fourth transistor coupled between a power supply and the first node~~ first potential is ground.

11. (currently amended) A clock buffer circuit to use with a scanning dynamic logic circuit comprising:

~~a series connection of transistors coupled between a first node and ground, the series connection of transistors including at least a first transistor and a second transistor, wherein the first transistor has a first control node coupled to receive a first signal corresponding to a functional clock and the second transistor has a second control node;~~

~~a logic circuit coupled to the second control node and coupled to receive the first signal and a first input; and~~

~~a third transistor coupled to the first node and having a third control node coupled to receive a second input~~

at least one clock generation circuit to generate one of a plurality of clock signals to the scanning dynamic logic circuit to allow the scanning dynamic logic circuit to scan in a test value, propagate the test value and obtain a resultant scanned sample output at an

output of the scanning dynamic logic circuit to perform a dynamic scan, the clock circuit including a first and second programmable transistors wherein a first input is to be coupled to a gate of the first transistor and a second input is to be coupled to a gate of the second transistor; and

an output node coupled to the transistors wherein selection of signals to the first and second inputs to the transistors determine if a first clock signal is to control a precharge cycle of a first stage of the scanning dynamic logic circuit, a second clock signal is to control an evaluate cycle of the first stage of the scanning dynamic logic circuit or a third clock signal is to control both precharge and evaluate cycles of subsequent stages of the scanning dynamic logic circuit to generate the output from the scanning dynamic logic circuit.

12. (currently amended) The clock buffer circuit as recited in claim 11 wherein the first input and the second input are coupled to ground to generate the third clock signal.

13. (currently amended) The clock buffer circuit as recited in claim 11 wherein the first input is coupled to ground and the second input is coupled to a scan mode signal indicative of whether or not scan is active to generate the second clock signal.

14. (currently amended) The clock buffer circuit as recited in claim 11 wherein the first input is coupled to a scan mode signal indicative of whether or not scan is active and the second input is coupled to ground to generate the first clock signal.

15. (currently amended) The clock buffer circuit as recited in claim 11 wherein the ~~series connection of transistors further comprises a fourth transistor having a fourth control node coupled to receive a condition signal~~ first input is coupled to a scan clock that clocks to scan in the test value and the second input is coupled to a scan mode signal indicative of whether or not scan is active to generate the third clock signal.

16-17. (canceled)

18. (currently amended) ~~In an apparatus including a first dynamic logic circuit having an output node on which a scan value is provided during scan and one or more second dynamic logic circuits, wherein one of the second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, the~~ A method comprising:

~~generating at least one evaluate pulse on a first clock controlling at least evaluation of the second dynamic logic circuits~~

generating a first clock signal to control a precharge cycle of a first stage of a scanning dynamic logic circuit;

generating a second clock signal to control an evaluate cycle of the first stage of the scanning dynamic logic circuit;

generating a third clock signal to control both precharge and evaluate cycles of subsequent stages of the scanning dynamic logic circuit;

isolating ~~the output~~ scan input node of the first stage of the dynamic logic circuit ~~from inputs to the first dynamic logic circuit using the second clock and the third clock responsive to a scan mode signal indicating that scan is active, the second clock controlling precharge of the first dynamic logic circuit and the third clock controlling evaluation of the first dynamic logic circuit~~ by using the first and second clock signals to control the precharge and evaluate cycles of the first stage of the scanning dynamic logic circuit;

inputting a scan test value;

propagating the test value through the subsequent stages by using the third clock signal; and

sampling the output of the ~~second~~ scanning dynamic logic circuits ~~subsequent to generating the at least one evaluate pulse, the output responsive to the scan value on the output node of the first dynamic logic circuit~~ to obtain a result of a scan operation.

19. (currently amended) The method as recited in claim 18 further comprising controlling ~~precharge of the second dynamic circuits using the first clock~~ the generation of the first, second and third clock signals by selecting different input locations for a scan mode signal which is used to activate the scan operation.

20. (currently amended) A computer accessible medium comprising one or more data structures representing:

a ~~first~~ scanning dynamic logic circuit ~~having an output node on which a scan value is provided during scan~~ arranged serially to scan in a test value, in which the test value is to be scanned into a dynamic node of a first stage, propagated through subsequent stages and a resultant scanned sample output to be obtained from an output stage of the scanning dynamic logic circuit; and

~~one or more second dynamic logic circuits, wherein one of the second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, and wherein an output of the second dynamic logic circuits is sampled in response to the scan value during scan~~

a clock buffer circuit coupled to the scanning dynamic logic circuit to generate a first, second and third clock signals in response to a scan clock signal to clock a scan operation and a scan mode signal to indicate activation of the scan operation; wherein the first clock signal is to control a precharge cycle of the first stage, the second clock signal is to control an evaluate cycle of the first stage and the third clock signal is to control both precharge and evaluate cycles of remaining stages of the scanning dynamic logic circuit, the first and second clock signals to isolate the first stage from dynamic operation while the subsequent stages dynamically propagate the test value.